LISTING OF THE CLAIMS

1. (Currently amended) A method of controlling a processor comprising consulting a table that lists a plurality of operation points defined by combinations each comprising: a) ~~switching parallel availability of~~ the number of ~~a plurality of~~ processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature.

2. (Canceled)

3. (Currently Amended) The method of controlling a processor according to claim 1, comprising allocating tasks in consideration of the number of the ~~plurality of~~ processing blocks available in parallel, the number being determined task by task.

4. (Currently Amended) The method of controlling a processor according to claim 1, comprising allocating tasks to at least a processing block having a lowest temperature among the ~~plurality of~~ processing blocks.

5. (Currently amended) A method of controlling a processor comprising consulting a table that lists a plurality of operation points defined by combinations each comprising: a) ~~switching between combinations of parallel availability of~~ the number of ~~a plurality of~~ processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points ~~and an operating frequency by consulting a predetermined table~~.

6. (Currently amended) The method of controlling a processor according to claim 5, wherein the table ~~describes~~ lists the plurality of operation points in the order of processing performance ~~for each of the combinations~~.

7. (Currently amended) The method of controlling a processor according to claim 6, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, ~~a combination~~ an operation point yielding a smaller amount of heat generation than that of ~~a combination~~ an operation point selected currently is detected out of the ~~combinations~~ operation points, so that the ~~combination~~ operation point selected currently is switched to the ~~combination~~ operation point detected.

8. (Currently amended) The method of controlling a processor according to claim 7, wherein when a plurality of ~~combinations~~ operation points are detected, the ~~combination~~ operation point selected currently is switched to a ~~combination~~ operation point yielding maximum performance.

9. (Currently amended) A processor comprising:

a plurality of processing blocks;

a sensor which measures a temperature; ~~and~~

a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit which consults the table and switches between the operation points ~~switches parallel availability of the plurality of processing blocks~~ in accordance with the measured temperature.

10. (Canceled)

11. (Original) The processor according to claim 9, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

12. (Original) The processor according to claim 9, wherein the control unit allocates tasks

to at least a processing block having a lowest temperature among the plurality of processing blocks.

13. (Currently amended) A processor comprising:

a plurality of processing blocks;

a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching ~~describes combinations of parallel availability of the plurality of processing blocks and an operating frequency~~; and

a control unit which consults the table and switches between the ~~combinations~~ operation points as appropriate.

14. (Currently amended) The processor according to claim 13, wherein the table ~~describes~~ lists processing performance for each of the combinations.

15. (Currently amended) The processor according to claim 14, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, the control unit selects ~~a combination~~ an operation point yielding a smaller amount of heat generation than at present out of the ~~combinations~~ operation points, and switches to the ~~combination~~ operation point selected.

16. (Currently amended) An information processing apparatus comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a sensor which measures a temperature~~; and~~

a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit which consults the table and switches between the operation points ~~switches parallel availability of the plurality of processing blocks~~ in accordance with the measured temperature.

17. (Canceled)

18. (Original) The information processing apparatus according to claim 16, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

19. (Original) The information processing apparatus according to claim 16, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

20. (Currently amended) An information processing apparatus comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching ~~describes combinations of parallel availability of the plurality of processing blocks and an operating frequency~~; and

a control unit which consults the table and switches between the ~~combinations~~ operation points as appropriate.

21. (Currently amended) An information processing system comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a sensor which measures a temperature; and

a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit which consults the table and switches between the operation points switches parallel availability of the plurality of processing blocks in accordance with the measured temperature.

22. (Currently amended) The information processing system according to claim 21, wherein the control unit switches between combinations of the parallel availability and an operating frequency the operation points in accordance with the temperature.

23. (Original) The information processing system according to claim 21, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

24. (Original) The information processing system according to claim 21, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

25. (Currently amended) An information processing system comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching describes combinations of parallel availability of the plurality of processing blocks and an operating frequency; and

a control unit which consults the table and switches between the combinations operation

points as appropriate.

26. (Currently amended) A processor readable storage medium having stored thereon a processor control program comprising instructions for:

consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor in operation; and b) one of a plurality of operating frequencies available for use by switching, and

switching ~~parallel availability of a plurality of processing blocks formed inside a processor~~ between the operation points in accordance with a temperature.

27. (Canceled)

28. (Currently Amended) The processor readable storage medium ~~processor control program~~ according to claim 26, further comprising instructions for allocating tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

29. (Currently amended) The processor readable storage medium ~~processor control program~~ according to claim 26, further comprising instructions for allocating tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

30. (Currently amended) A processor readable storage medium comprising a processor control program comprising instructions for:

consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor in operation; and b) one of a plurality of operating frequencies available for use by switching, and

switching between the operation points ~~between combinations of parallel availability of a plurality of processing blocks formed inside a processor and an operating frequency by consulting a predetermined table~~.

31. (Previously presented) The method of controlling a processor according to claim 3, comprising allocating tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

32. (Previously presented) The processor according to claim 11, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

33. (Previously presented) The information processing apparatus according to claim 18, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

34. (Previously presented) The information processing system according to claim 23, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing tasks.

35. (Currently amended) The processor readable storage medium ~~processor control program~~ according to claim 28, further comprising instructions for allocating tasks to at least a processing block having a lowest temperature among the plurality of processing tasks.